Spring 2019

California State University, Northridge

Department of Electrical & Computer Engineering

Lab Experiment 2

Structural Modeling of a JK Flip-Flop

(*Late*)

February 14, 2019

ECE 526L

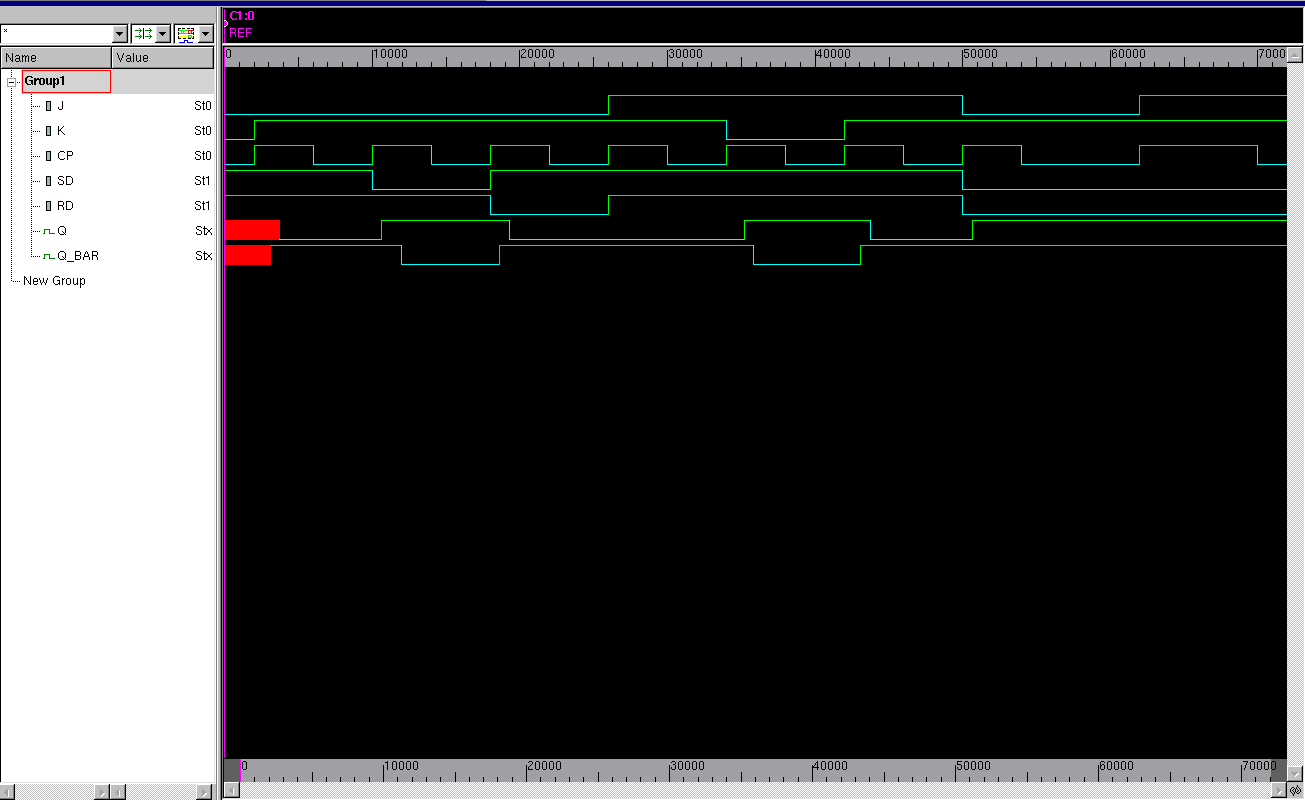
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**Introduction:**

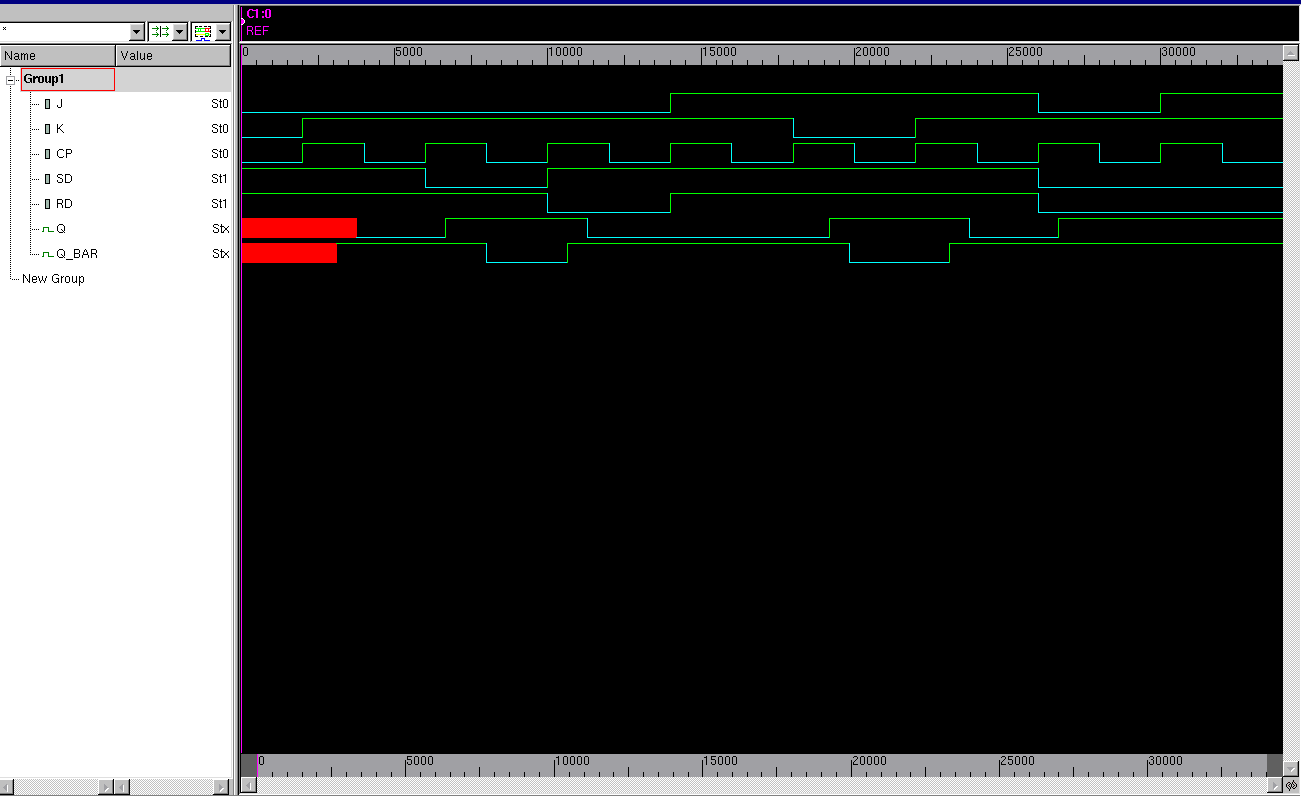
In this experiment, a JK flip-flop will be constructed with combinational logic using structural modeling. Gate delays will be incorporated due to factors such as fan-in and fan-out delay. Primitives will be used in stages to design each stage of the JK flip-flop. A testbench will be used to verify that the JK flip-flop will function correctly. A small set of vectors are used as inputs and the outputs are observed to see if the flip-flop functions correctly.

**Procedure:**

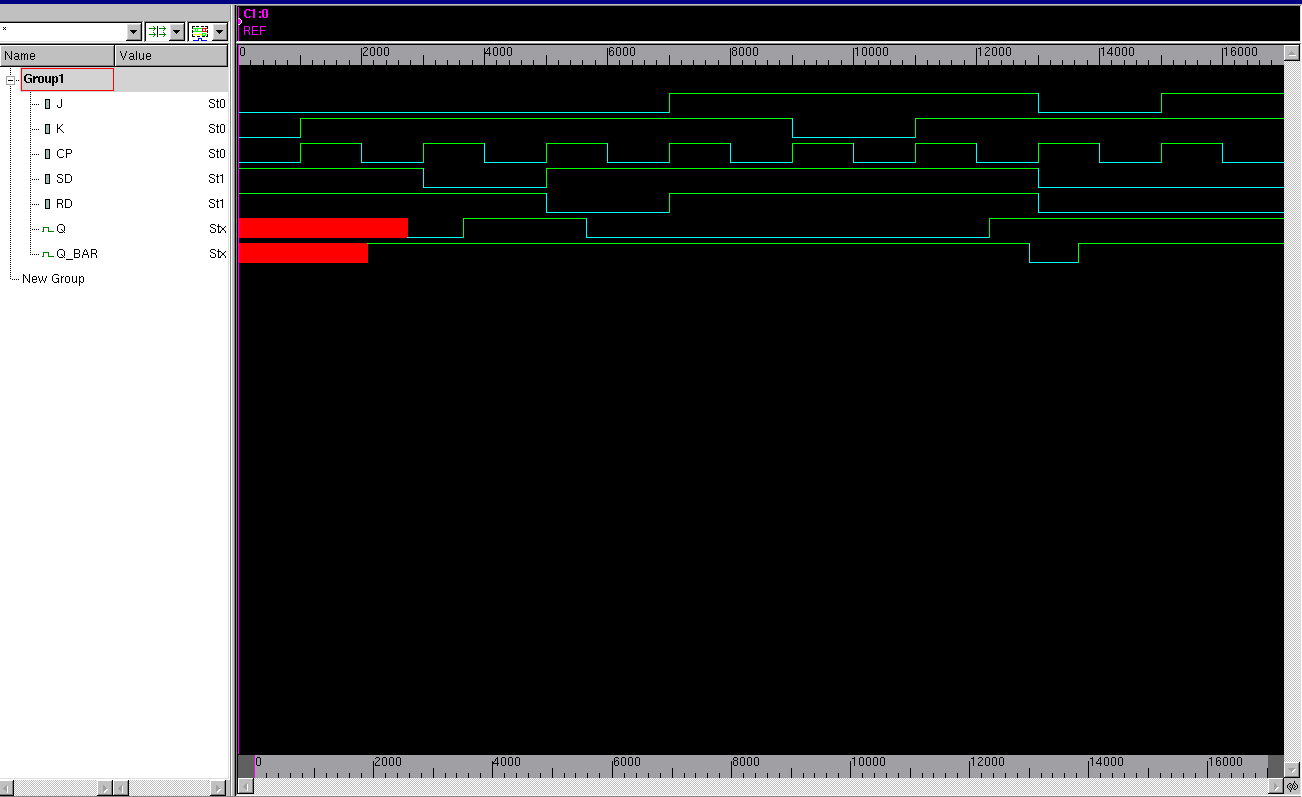
1. A JK flip flop can be constructed in four stages. Each stage will receive an input and the output of that stage will serve as a input to the next stage. Using a combination of primitive gates will create a five input flip flop and produce two outputs.
2. Delay times are considered to allow sufficient time for the input changes to propagate throughout the circuit. In the module, delays are added in each stage based in its fan-in and fan-out. A define directive is used to modify any delays if the delay values were to change.
3. A testbench is created to test the functionality of the JK FF. A minimal number of vectors can be used to verify the function of the JK flip flop. It’s function is such that setting J will load a logic high value to Q. Setting the K value will load a logic low to Q. Setting both of the values to logic high will create a toggle and setting them both to low will simple hold the current value of Q.
4. The output of the testbench will tested using various duty cycles to see the change in behavior of the circuit as the interval between the positive edge and the negative edge decreases for each duty cycle change. The maximum operating frequency will be calculated and compared to the simulated frequency.

**Results:**  


***Figure 1.1*** *- Simulated Waveform of JK Flip Flop*

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***Figure 1.2*** *- Simulated Waveform with 50% duty cycle*

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***Figure 1.3*** *- Simulated Waveform with 10% duty cycle*

**Discussion:**

When assigning the initial conditions for the JK FF, the inputs will be unknown. It will take some time before the output will reach a steady state. Both Q and Q\_BAR will not change at the same time. This is because the unknown outputs will also be used as inputs in primitive gate level. Therefore, it will take time before Q and Q\_BAR will be assigned a logical value due to the gate delays for each stage of the structural model for the JK FF. These stages are outputs of one gate going into the input of another stage. To test for the indeterminate state, two identical tests were done to see if there is a consistent output. However, an indeterminate state is unpredictable because the output is unknown. This is demonstrated in *Figure 1.2* where the output has an equal Q and Q\_BAR. The output Q takes on one of two values based on the active low inputs SD and RD since they are both set. Therefore, both Q and Q\_BAR are trying to be set and reset and the same time and the result comes from the race between a set and reset.

The amount of time to allow for each input is provided by the fan-in and fan-out delay. The input delay was calculated to be 8 ns for the first stage, 7 ns for the second stage, 10 ns for the third stage, and 13 ns for the final stage with a total of a 40 ns delay. The theoretical operating frequency will be the inverse of the propagated delay which is 2.50 MHz. In comparison, to the simulated circuit will has a maximum delay of 340 ns with a frequency of of 2.94 MHz. Based on the simulation, more delays occur if the clocks are at a 50% duty cycle as the the setup and hold time for each stage of the JK flip flop have less time with half the clock interval. The maximum delay for a 10% duty cycle will be 0.85 ns which result in a maximum frequency of 11 Ghz. Although the circuit is running at a fast rate, the JK FF will not function as intended since there is no time for the inputs to change state with a faster clock interval.

**Conclusion:**

Structural modeling is used to create a system of primitive gates to build larger components. With multiple levels of gates, the output of one level will be the input of another system. This introduces gate delays and are calculated using fan-in and fan-out delay propagation. This propagation is necessary for functionality of the component to allow the clock to perform synchronously which is important in sequential circuit designs. From this experiment, this delay is taking into account to allow all inputs to be in a steady state before the next clock signal. Otherwise, the circuit is not synchronous and will not behave as a sequential circuit.